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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,833	12/29/2003	Matthew B. Harris	INSL.0089	6190

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EXAMINER	
RILEY, SHAWN	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,833	HARRIS ET AL.	
	Examiner	Art Unit	
	Shawn Riley	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-15* is/are allowed.

6)☒ Claim(s) *1-3 and 16-20* is/are rejected.

7)☒ Claim(s) *4-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *dec 03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawing(s) is(are) objected to because they fail to label (figure(s) 1-3) what the elements 103, 105 and element boxes 107 are. Without some indication as to the content of the boxes (or preferably ansi symbols of the actual elements) it is not clear as to what the elements are and they are not explanatory to a reader as a quick method of determining the general background of the invention.

See MPEP 608.02 and 37 CFR 1.84 (o) -- **Legends**

Suitable descriptive legends may be used, or may be required by the Examiner, where necessary for understanding of the drawing, subject to approval by the Office. They should contain as few words as possible.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Clocked Cascading Current-Mode Regulator (titles should not list improvements).

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 3718 of this title before the invention thereof by the applicant for patent.

2. Claims 1-3 are rejected under 35 U.S.C. §102(e) as being fully anticipated by Kates et al. (U.S. Patent 6,218,815). Kates et al. shows,[1] (in, e.g., the(ir) figures 1-3 and corresponding disclosure)

As to claim 1;

A clocked cascadable power regulator (see, e.g., figure 1), comprising: synchronization logic (e.g., including 104 in figure 1 and 201-234 in figure 2A) that receives a clock signal (CLK) and that asserts a digital output signal (EN_n) synchronized with said clock signal in response to assertion of a digital input signal (could either be Q*A Q*B, QA, QB or input from node B at figure 2A or input C_{PULSE} in figure 2a, e.g.,); and PWM control logic (e.g., 241/242/243/244/245/246 and likewish 251/252/250/253/254/255/256, etc.) that controls each PWM cycle in response to said digital input signal (through circuitry) and an output control condition (e.g., in figure 2B, the feedback signal of V_{OUT} compared in 295 and fed through node B back into circuitry):

1 Note claims will be addressed individually and the material in parentheses are the examiner's annotated comments. Further unless needed for clarity reasons, recited limitation(s), will be annotated only upon their first occurrence. Annotated claims begin with the phrase "As to claim". Claims that are not annotated are seen as having already had the invention(s) addressed previously in an annotated claim. Bolded words/phrases indicate rejected material based 112 paragraph rejections. Underlined words/phrases indicate objected to material.

2. The clocked cascadable power regulator of claim 1, wherein said PWM control logic comprises: PWM logic that initiates a PWM cycle in response to said digital input signal and that terminates said PWM cycle in response to a reset signal (reset signal produced by AND circuits 241/251/261/271, see, e.g., column 6 lines 34-40); and feedback sense logic, coupled to said PWM logic, that asserts said reset signal when said output control condition is met (reset signal is asserted through node B to same set of AND circuits based on Vout).

3. The clocked cascadable power regulator of claim 2, wherein said PWM logic comprises: a latch (242/252/262/272) that sets in response to said digital input signal and that resets in response to said reset signal; gate control logic (inside 242), coupled to said latch, that provides at least one PWM activation signal (Q/Qnot); and at least one driver amplifier (243/244), each responsive to said at least one PWM activation signal.

For method claims, note that under MPEP 2112.02, the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). Therefore the previous rejections based on the apparatus will not be repeated.

16. A method of controlling each of a plurality of clocked cascadable regulators of a multiphase converter, comprising: coupling a digital output of each regulator to a digital input of another regulator; providing a common clock signal to a clock input of each regulator; providing a digital output signal on the digital output synchronized with the common clock signal in response to receiving a digital input signal at the digital input; and controlling a PWM cycle in response to receiving the digital input signal and in response to detecting an output condition.

17. The method of claim 16, further comprising programming a switching frequency FSW of the multiphase converter with N regulators by programming the frequency of the common clock signal to N*FSW.

18. The method of claim 16, further comprising: detecting an output current condition and generating a sense signal; and comparing the sense signal with a compensation signal.

19. The method of claim 18, wherein said detecting an output current condition comprises detecting peak current through an output inductor.

20. The method of claim 18, further comprising providing a central controller that senses an output voltage condition and that provides the compensation and clock signals to each regulator.

Allowable Subject Matter

3. Claims 4-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 8-15 are allowable over the prior art of record.

5. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and section 707.07(a) of the M.P.E.P.

6. The following is an examiner's statement of reasons for allowance: No prior art uncovered anticipates or renders obvious applicant(s) claimed a plurality of regulators coupled in a cascade configuration, having synchronization logic receiving a clock signal and a digital start input signal from a previous regulator and that provides a digital start output signal to a next regulator in response to said digital start input signal and synchronized with said clock signal; and PWM control circuit that controls a PWM output in response to assertion of said digital start input signal and based on meeting an output condition; a plurality of switching circuits, each having an input coupled to a PWM output of a corresponding one of said plurality of regulators, an output for driving a common DC output voltage, and a sense output provided to a PWM control circuit of said corresponding regulator; and a controller that senses said DC output voltage and that provides a compensation signal to said PWM control circuit of said corresponding regulator and that provides said clock signal.

Further prior art uncovered anticipates or renders obvious applicant(s) claimed circuitry including id feedback sense logic including a sense amplifier that senses an output current condition and that asserts a sense signal; and a comparator that compares said sense signal with a feedback reference signal to determine said output control condition. Further prior art uncovered anticipates or renders obvious applicant(s) claimed circuitry including startup logic that disables synchronous cascaded operation during initialization. Further prior art uncovered anticipates or renders obvious applicant(s) claimed circuitry including synchronization logic includes comprises cascaded flip-flops responsive to said clock signal and said digital input signal.

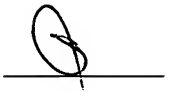
Further prior art uncovered anticipates or renders obvious applicant(s) claimed circuitry including a weak pull-down device coupled to pull-down said digital output signal unless otherwise driven high by a digital output signal from another regulator.

Conclusion

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Mike Sherry who can be reached at 571.272.2084. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number 703.872.9306. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at http://pair-direct.uspto.gov wherein unpublished application information is found through private PAIR and published application information is

found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

April 05



Shawn Riley

Primary Examiner